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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,918	07/09/2001	Ken Fernald	CYGL-24,692	7118

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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,918	FERNALD, KEN	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 11, 2006 has been entered.

2. Claims 1-14 are presented for examination.

3. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

4. The rejection of claim 7 under 35 U.S.C. 112 first paragraph is hereby withdrawn due to amendment filed June 11, 2006.

5. The rejection of claims 1-14 under 35 U.S.C. 112 second paragraph is hereby withdrawn due to amendment filed June 11, 2006.

Claim Objection

6. Claims 8-14 are objected to under 37 CFR 1.75(b) as not

substantially differing from claims 1-7.

The claims as written do not appear to be substantially different or to provide substantially different patent protection.

Applicants are required to ***1) cancel the objected to claims, (2) amend the claims so that they are substantially different from any other claims, or (3) provide sufficient reasons why the claims as presently written are substantially different or provide substantially different patent protection.***

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotley (US Patent # 5,442,704) and Zimmer et al. (US Patent # 6,633,964).

9. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotley (US Patent # 5,442,704) and Sharma et

al. (US Patent # 6,636,906).

10. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotley (US Patent # 5,442,704) and Wolrich et al. (US Patent # 6,681,300).

With respect to claims 1 and 8, Hotley discloses:

storing in a location in memory on one of the logical portions thereof a plurality of lock bits, each of the lock bits associated with a separate one of the logical portions of the memory space and determinative as to the access thereof for a predetermined memory access operation thereon, as shown by the lock bits (item 54a) located in a separate logical column, for each row(54b) of the memory array in figure 4;

detecting a request for access to a desired location in the memory space for operating thereon, as shown in figure 6b;

comparing the requested memory access operation with the associated lock bit in the associated logical portion and determining if access is allowed for the requested memory access operation, and performing the requested memory access operation if allowed, as shown by protection determination and ensuing execution starting in step 626 in figure 6b;

there being at least two different memory access operations, as taught in column 9, lines 2-6.

With respect to claims 2 and 9, Hotley discloses the operation being a read of an addressable location, as recited in

column 9, lines 2-6.

With respect to claims 3 and 10, Hotley discloses the operation being a write of an addressable location, as recited in column 9, lines 2-6.

With respect to claims 4 and 11, Hotley discloses the operation being an erase of the associated logical portion of an addressable location therein, by teaching in column 9, line 25, of a block erase operation.

With respect to claims 5 and 12, Hotley discloses:

storing the plurality of lock bits in a variable location in the memory and storing the location of the lock bits in a known location in the memory, as shown by one lock bit being stored for each row of memory in figure 4;

in the step of comparing, the location of the lock bits is first read from the known location in memory and then this read location is utilized to read the lock bits are read from memory by teaching in column 13, lines 24-35, that each step instruction causes the middle address bits stored in the address latch counter 30-3 to be incremented by one for readout of the next lock bit location LMBI, then contents of the location LMBI is compared with the key bit presented by ACP 10 which is the first key bit of the sequence to be compared.

With respect to claims 6 and 13, Hotley discloses the predetermined operation being an erase of the lock bits, by teaching in column 11, lines 10-15, that when a block is erased,

all of its data including the lock bits stored in the lock storage area are set to ONES.

With respect to claims 7 and 14, Hotley discloses the operation of erasing the lock bits requires that each of the lower logical portions with lower logical portions of the memory space relative to the variable location and not containing lock bits to be erased before the top most portion with higher logical addresses that contains the lock bits, by teaching in column 14, lines 15-20, of an erase being performed on the block designated by the most significant bits contained in the counter.

With respect to claims 1 and 8, Hotley teaches all other limitations, as discussed above, but fails to specifically disclose using the lock bits to determine if the requested predetermined type of access is allowed.

Zimmer et al. teach in figure 2B and column 4, lines 40+, of both a read lock bit and a write lock bit which would lock access to the memory block for either a read access type or a write access type.

It would have been obvious to one of ordinary skill in the art, having the teachings of Hotley and Zimmer et al. before him at the time the invention was made, to modify the lock bits taught by Hotley, to include separate lock bits for both read and write access types, as with the lock bits of Zimmer et al., in order to prevent undesired memory accesses and possible data loss/corruption, ms taught by Zimmer et al.

Sharma et al. teach in figure 3, of a read lock bit which would lock access to the memory block from a predetermined access type, wherein the access type locked is a read.

It would have been obvious to one of ordinary skill in the art, having the teachings of Hotley and Sharma et al. before him at the time the invention was made, to modify the lock bits taught by Hotley, to include a read lock bit, as with the lock bits of Sharma et al., in order to prevent undesired read type memory accesses and possible data loss/corruption, as taught by Sharma et al..

Wolrich et al. teach in figure 3, of a read lock bit which would lock access to the memory block from a predetermined access type, wherein the access type locked is a read.

It would have been obvious to one of ordinary skill in the art, having the teachings of Hotley and Wolrich et al. before him at the time the invention was made, to modify the lock bits taught by Hotley, to include a read lock bit, as with the lock bits of Wolrich et al., in order to prevent undesired read type memory accesses and possible data loss/corruption, as taught by Wohich et al.

27. With respect to the independent claims, the Applicant alleges that the lock bits in Hotley are not contained in a separate logical portion of the memory space.

28. With respect to the independent claims, the Applicant

alleges that the lock bits in Zimmer, Sharma, and Wolrich, are not contained in a separate logical portion of the memory space, but are in separate memory device altogether. The claims, though, do not limit the memory space to a single physical medium. Only a separate logical portion of the memory space is claimed. As such, a separate physical memory medium logically associated with the data array would read upon the claim language.

11. As per remark, Applicant's counsel asserts that (a) "Hotley stores the memory locations in an area of the memory that cannot be protected, i.e., the lock byte protects itself." (amendment, page 6, fourth paragraph).

First of all, it should be noted that Hotley discloses the stored memory locations can be protected wherein Hotley's figure 4 again shows the lock bits in a separate logical column from the rest of the data bits. In addition; in considering a 35 USC 103 rejection, it is not strictly necessary that a reference or references explicitly suggest the claimed invention (this is tantamount to a 35 USC 102 reference if the modifications would have been obvious to those of ordinary skill in the art. It has been held that the test of obviousness is not whether the features of a secondary reference may be bodily incorporated into the primary references' structure, nor whether the claimed invention is expressly suggested in any one or all of the

references; rather, the test is what the combined teachings of the reference would have suggested to those of ordinary skill in the art. See In re Keller et al., 208 U.S.P.Q 871. In addition, Examiner further recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). Zimmer et al., Sharma et al., Wolrich et al. and Hotley references are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969. In this case, the Zimmer et al., Sharma et al., Wolrich et al. references were used to provide evidence of separate lock bits are utilized for both read and write access type which is known to be required in the system of Hotley in order to arrive at Applicant's current invention. The 35 USC § 103 rejection based on said combination is therefore deemed to be proper.

Conclusion

12. Any inquiry concerning this communication or earlier

communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see ***http://pair-direct.uspto.gov***. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/August 18, 2006

Tuan V. Thai
PRIMARY EXAMINER
Group 2100